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09/808,484	03/14/2001	Kelly T. Hurley	MIO 0064 PA	3606

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/808,484	Applicant(s) HURLEY ET AL.	
	Examiner Kevin Quinto	Art Unit 2826	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) *1-11,13-18,23,26-32,35,39,41-72,75 and 77-90* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,19-22,24,25,33,34,36-38,40,73,74 and 76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. The applicant states that claims 9-11 read on figure 2. However the examiner believes that this is not the case. Claim 9 contains the limitation "at least one ear formed adjacent to said at least one floating gate layer and over a portion of said field oxide region." Figure 2 does not have an ear which is formed *over* a portion of the field oxide region; the ear is formed adjacent to the field oxide region. Therefore claims 9-11 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

2. The applicant states that claim 35 reads on figure 2. However the examiner believes that this is not the case. Claim 35 contains the limitation "wherein the ear is in proximity of, but not in contact with the field oxide." Figure 2 has an ear which is *in contact with the field oxide*. Therefore claim 35 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

3. In the prior Office action, claims 73-75 were withdrawn from further consideration. This is an error. However the applicant does appear to be aware of this since claims 73 and 74 were elected for examination.

4. Claims 41-71, 77-82, 85 and 86 were withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention in the prior Office action.

5. Claims 1-8, 13-18, 23, 26-32, 39, 72, 75, 83, 84, and 87-90 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

7. Claim 40 is objected to because of the following informalities: the phrase "a conductive bit line connecting connected to the drain of each memory cell of the row" is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 20-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 20 recites the limitation "polysilicon wings" in the third line. There is insufficient antecedent basis for this limitation in the claim.

11. The examiner believes that the applicant is referring to the "polysilicon ears" as previously defined in claim 19 but is not certain.

12. Claim 21 recites the limitation "said floating gate" in the last two lines. There is insufficient antecedent basis for this limitation in the claim.

13. The examiner believes that the applicant is referring to the "floating gate layer" as previously defined within the claim.

14. Claim 22 recites the limitation "polysilicon wings" in the third line. There is insufficient antecedent basis for this limitation in the claim.

15. The examiner believes that the applicant is referring to the "polysilicon ears" as previously defined in claim 21 but is not certain.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 12, 19-22, 24, 25, 33, 34, 36-38, 73, 74, and 76 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong (USPN 5,770,501).

18. In reference to claim 12, figures 6a-6f of Hong (USPN 5,770,501) disclose a device which meets the claim. Figures 6a-6f illustrate a substrate (50) with at least one semiconductor layer (50). There is at least one trench formed in the substrate (50). There is a field oxide (542) inside the at least one trench and it extends above an upper surface of the substrate (50). A tunnel oxide layer (512) is formed over at least a portion of the substrate (50). There is at least one floating gate layer (514a) formed over the tunnel oxide layer (512). There is at least one polysilicon ear (552) formed on the at least one floating gate layer (514a) and is adjacent to the field oxide (542).

19. With regard to claim 19, figures 6a-6f of Hong disclose a device which meets the claim. Figures 6a-6f illustrate a substrate (50) with at least one semiconductor layer (50). There is a plurality of trenches formed in the substrate (50). A field oxide (542) is inside each of the trenches. A tunnel oxide layer (512) is formed over the substrate (50). A floating gate layer (514a) is formed over the tunnel oxide layer (512). A pair of polysilicon ears (552) are formed adjacent to the field oxide regions (542) on the floating gate layer (514a). The polysilicon ears (552) are projecting substantially perpendicular to the upper surface of the floating gate layer (514a).

20. So far as understood in claim 20, Hong meets the limitation of the claim. Figures 6a-6f shows that the floating gate layer (514a) comprises a plurality of floating gates and a corresponding pair of polysilicon ears for each of the plurality of floating gates.

21. So far as understood in claim 21, figures 6a-6f of Hong disclose a device which meets the claim. Figures 6a-6f illustrate a substrate (50) with at least one semiconductor layer (50). There is a plurality of trenches formed in the substrate (50). A field oxide (542) is inside each of the trenches. A tunnel oxide layer (512) is formed over the substrate (50). A floating gate layer (514a) is formed over the tunnel oxide layer (512). A pair of polysilicon ears (552) are formed adjacent to a portion of the floating gate (514a).

22. So far as understood in claim 22, Hong meets the limitation of the claim. Figures 6a-6f shows that the floating gate layer (514a) comprises a plurality of floating gates and a corresponding pair of polysilicon ears for each of the plurality of floating gates.

23. In reference to claim 24, figures 6a-6f and 7 of Hong (USPN 5,770,501) disclose a device which meets the claim. Figures 6a-6f and 7 illustrate a substrate (50) with at least one

semiconductor layer (50). There is at least one trench formed in the substrate (50). There is a source and a drain (572, both of them) formed in the substrate (50). There is a field oxide (542) inside the at least one trench and it extends above an upper surface of the substrate (50). A tunnel oxide layer (512) is formed over at least a portion of the substrate (50). There is at least one floating gate layer (514a) formed over the tunnel oxide layer (512). There is at least one polysilicon ear (552) formed on the at least one floating gate layer (514a) and is adjacent to the field oxide (542). There is a dielectric layer (562) formed over the substrate (50) and the floating gate layer (514a). There is a control gate layer (564(a)) formed over the dielectric layer (562).

24. In reference to claim 25, figures 6a-6f and 7 of Hong (USPN 5,770,501) disclose a device which meets the claim. Figures 6a-6f and 7 illustrate a substrate (50) with at least one semiconductor layer (50). There is at least one trench formed in the substrate (50). There is a source and a drain (572, both of them) formed in the substrate (50). A tunnel oxide layer (512) is formed over at least a portion of the substrate (50). There is at least one floating gate layer (514a) formed over the tunnel oxide layer (512). There is a field oxide (542) inside the at least one trench. There is at least one polysilicon ear (552) formed on the at least one floating gate layer (514a). There is a dielectric layer (562) formed over the substrate (50) and the floating gate layer (514a). There is a control gate layer (564(a)) formed over the dielectric layer (562).

25. With regard to claims 33 and 34, figures 6a-6f and 7 of Hong (USPN 5,770,501) disclose a device which meets these claims. Figures 6a-6f and 7 illustrate a device with a source and a drain (572, both of them) formed in a substrate (50). There is a floating gate (514a) formed over the substrate (50). There is a field oxide (542) formed in the substrate (50). There is a polysilicon ear (552) formed over the substrate (50). There is a dielectric layer (562) formed

over the substrate (50) and the floating gate layer (514a). There is a control gate layer (564(a)) formed over the dielectric layer (562).

26. In reference to claim 36, figures 6a-6f of Hong show that the ear (552) extends beyond the bounds of the floating gate (514a).

27. In reference to claim 37, figures 6a-6f of Hong show that the vertical sides of the ear (552) do not contact the floating gate (514a).

28. With regard to claim 38, figures 6a-6f of Hong show that the vertical edge of the ear (552) is adjacent to the field oxide (542) while the bottom edge of the ear (552) is adjacent to the floating gate (514a).

29. In reference to claims 73 and 74, figures 6a-6f of Hong (USPN 5,770,501) disclose a device which meets the claim. Figures 6a-6f illustrate a substrate (50) with a field oxide region (542) and a tunnel oxide layer (512). There is at least one floating gate layer (514a) formed over the tunnel oxide layer (512). There is at least one polysilicon structure (552) formed adjacent to the at least one floating gate layer (514a). This polysilicon structure or ear increases the capacitive coupling of the memory cell.

30. With regard to claim 76, figures 6a-6f of Hong shows that the polysilicon structure or ear is formed adjacent to the field oxide region (542).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong (USPN 5,770,501) in view of Yoo et al. (USPN 5,747,848).

33. In reference to claim 40, figures 5, 6a-6f and 7 of Hong (USPN 5,770,501) disclose a device which meets the claim. Figures 5, 6a-6f and 7 illustrate a substrate (50) with a source and a drain (572, both of them). It is understood that the source and the drain are formed in common regions with adjacent memory cells. There is a floating gate layer (514a) with a pair of polysilicon ears (552). There is a control gate (564(a)) associated with each row. Figure 5 shows that the control gate layer (564(a)) is formed as a common word line which is associated with each row. It is understood that the control gate is formed integral with the word line since Hong interchangeably uses the terms "control gate" and "word lines" (column 3, lines 48-51). Hong does not disclose the use of a conductive bit line which is connected to the drain of each memory cell in a row in conjunction with a common source line, otherwise known as the NOR configuration. However it is well known in the art to implement a flash memory in this manner. Yoo et al. (USPN 5,747,848) discloses that NOR-type devices have a higher speed than NAND-type devices (column 1, lines 28-32). It would therefore be obvious to implement the device of Hong with a common source line and a conductive bit line that is connected to the drain of each memory cell in a row in order to attain the benefit of a high speed memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
October 1, 2002

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